

Fig. 1

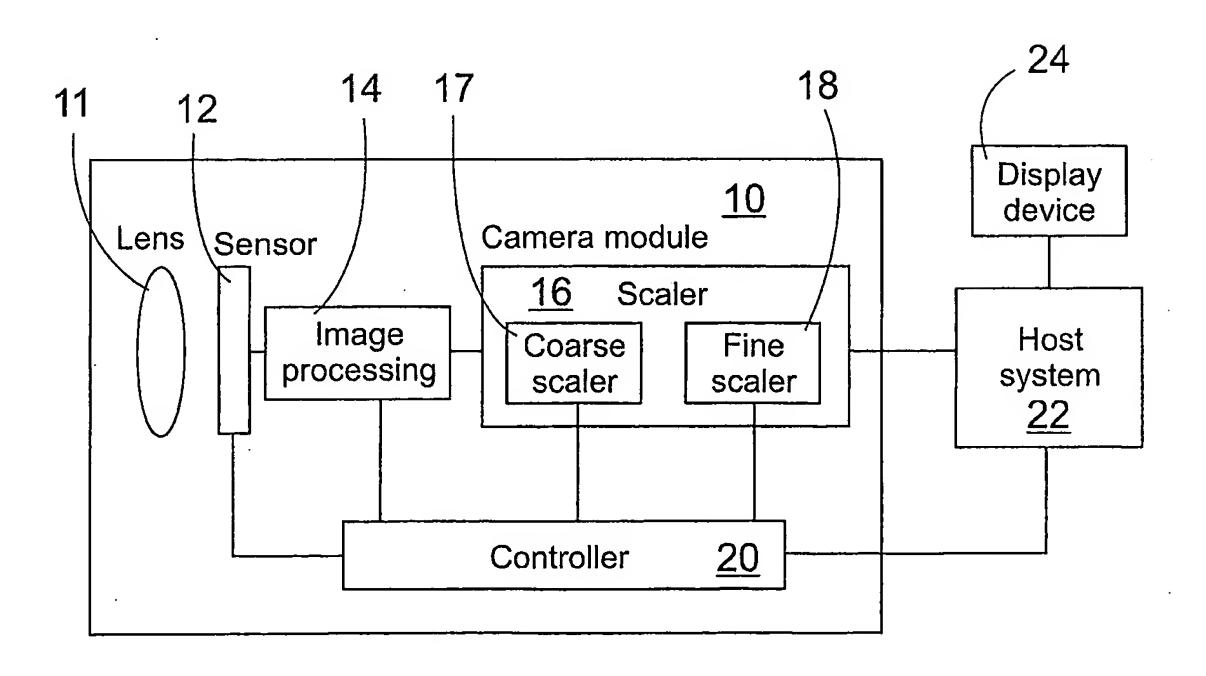


Fig. 2a

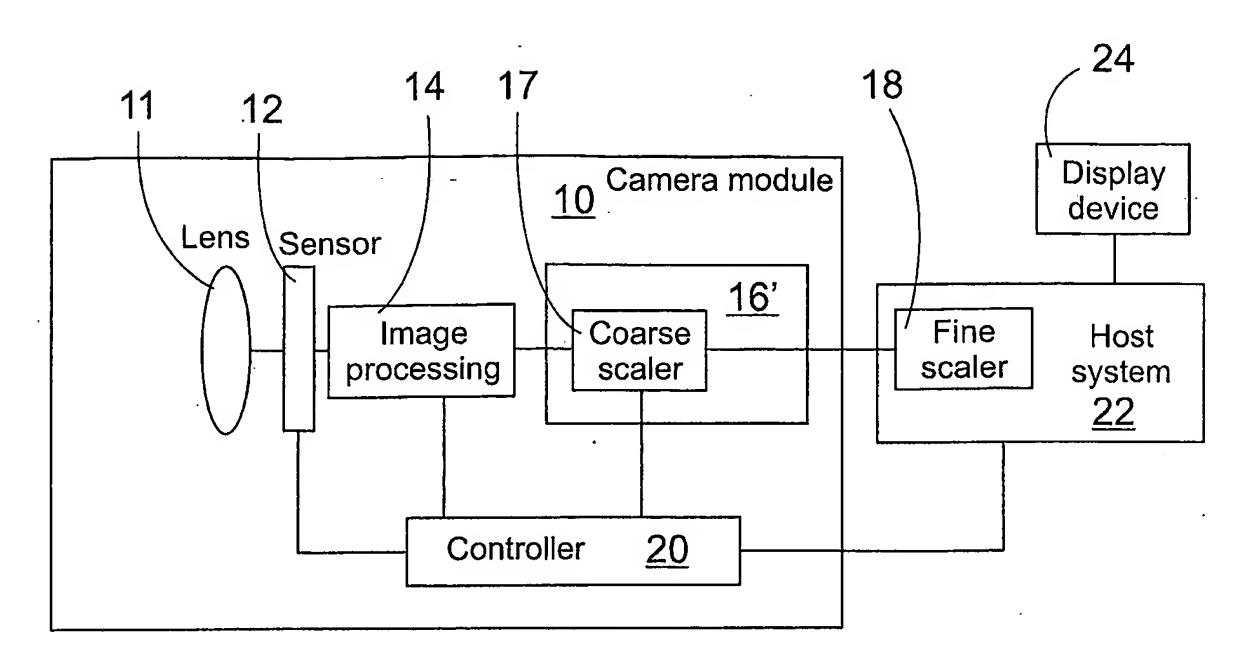
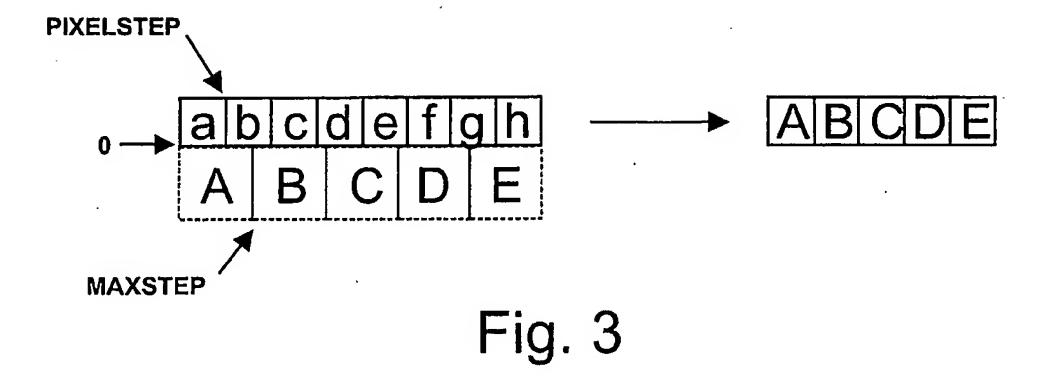
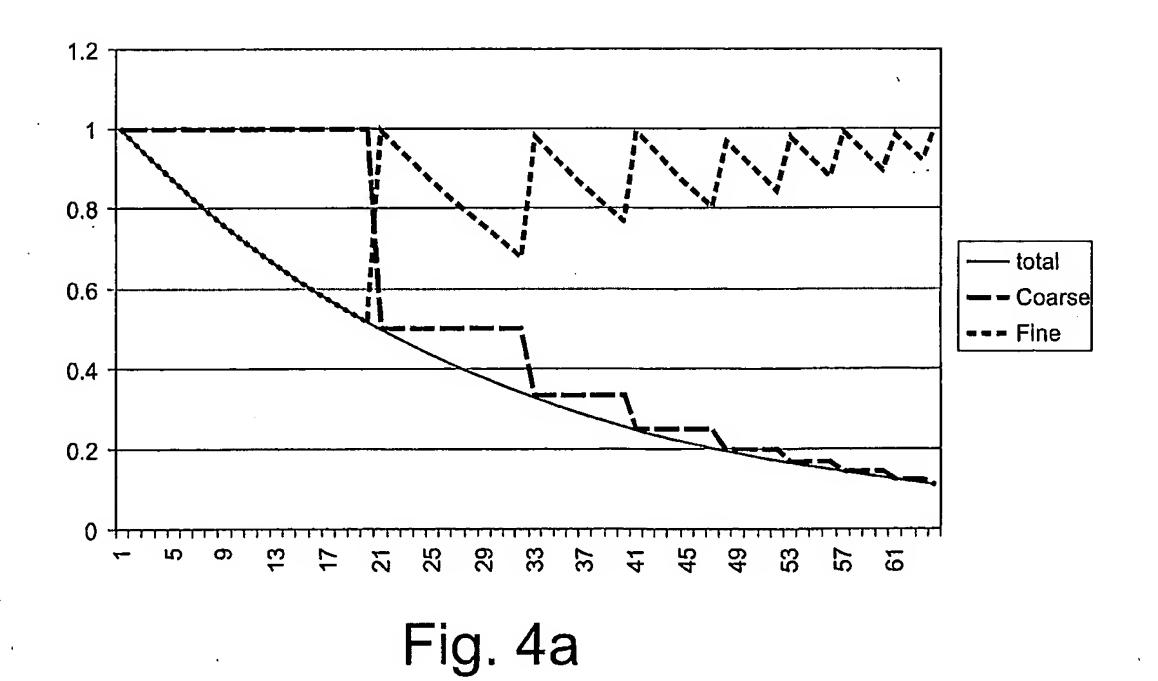


Fig. 2b 18 16' 163 162 183 <u>22</u> Host system <u>10</u> 182 ארן די Memory Memory CPU CPU Input unit Input unit Output Cutput 184 Control Control 181 · 164 161 165 185 187 167

Fig. 2c





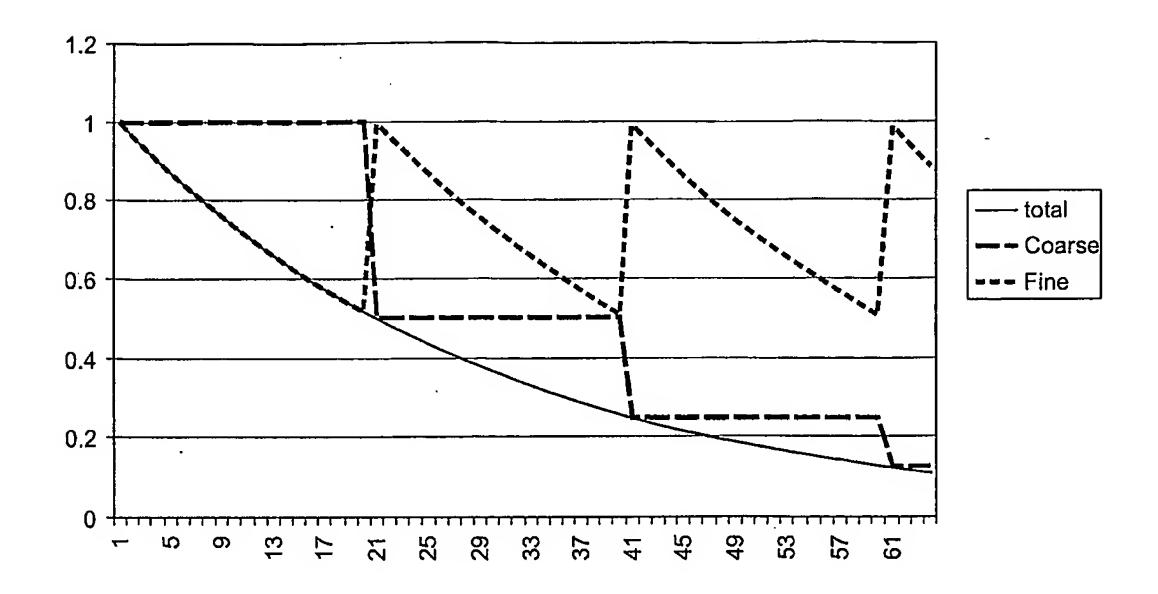


Fig. 4b

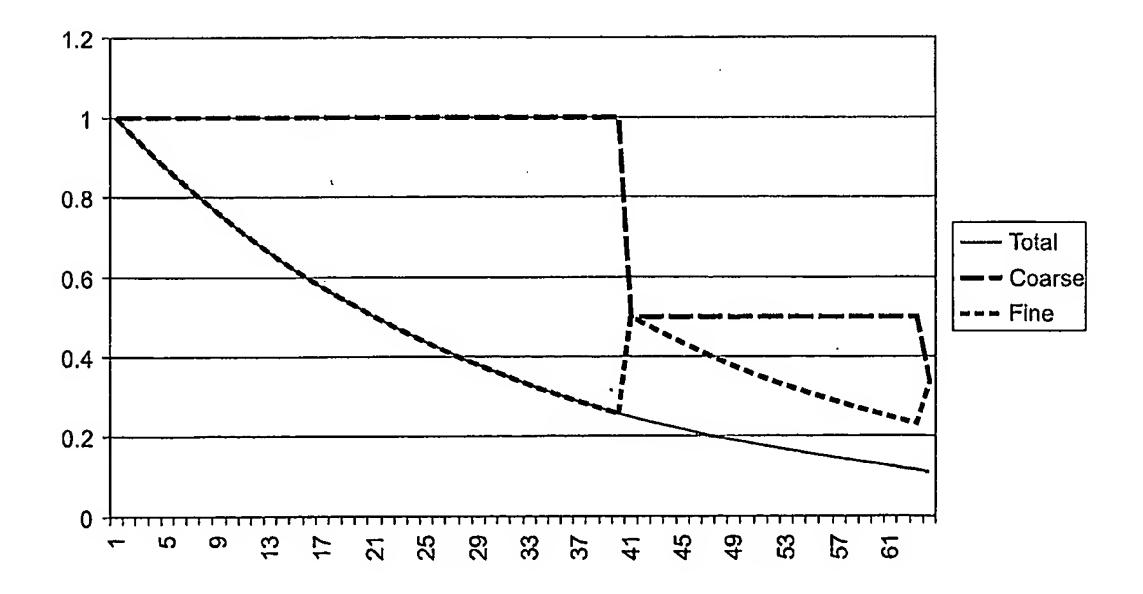


Fig. 4c